— NOTES —
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6 The Field Effect Transistor -- FET.

The FET is a unipolar device (the current flow is characterized by either the flow of negative carriers -- N Channel or the positive carriers -- P Channel) and can be considered as a voltage controlled device (the BJT Transistor is a current controlled device) .
The advantages of the FET are as follows :

1 - The FET has a very high input resistance (> 5 Mega ohms)
2 - The FET is less noise than the bipolar transistor , which makes it ideal for high quality Hi-Fi applications.
3 - The FET exhibits no offset voltage at zero drain current , which makes it ideal as signal chopper

The main disadvantage of the FET is it's small gain - band width compared with the conventional transistor .

6.1 The basic types of FETs .

There are two basic types of the FET :

(a) Junction FET or JFET
(b) Metal oxide semiconductor FET or MOSFET

6.1.1 The JFET

6.1.1.1 The basic construction of the JFET.

The basic construction of the JFET is as shown in Fig (6.1) . The diagram illustrate an N - Channel JFET which consists of a channel made from an N type semiconductor material with two metallic contacts (the Drain and the Source) at its end (the source and drain are interchangable). Also two P - Type semiconductor material are diffused (to form what is called the Gate) as shown . For a P - Channel JFET , the opposite semiconductor materials are employed .

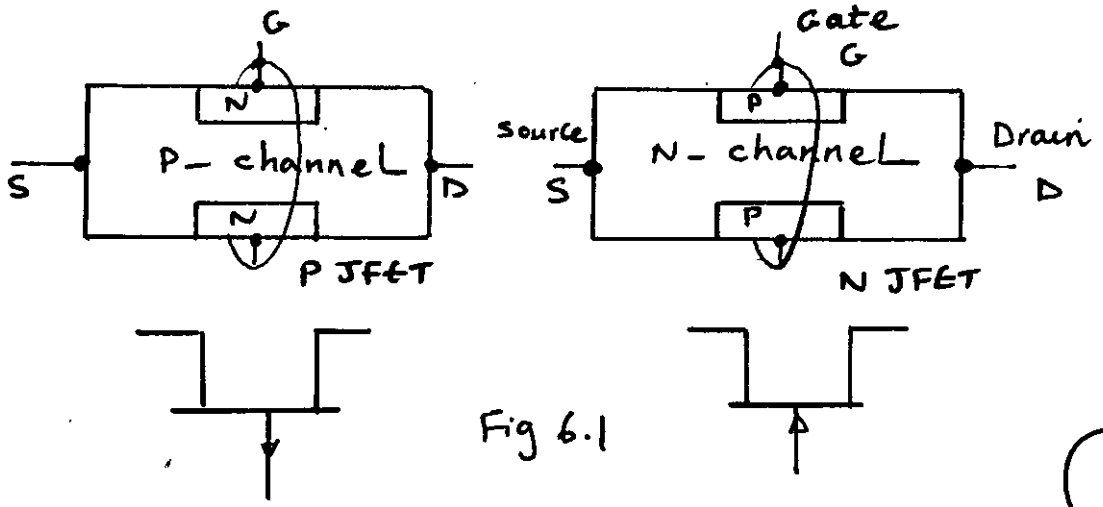


Fig 6.1

6.1.1.2 The operation and characteristics of the JFET .

The normal configuration of an N - Channel JFET (The P - Channel JFET is the same with voltages and currents are reversed) is as shown in Fig (6.2).

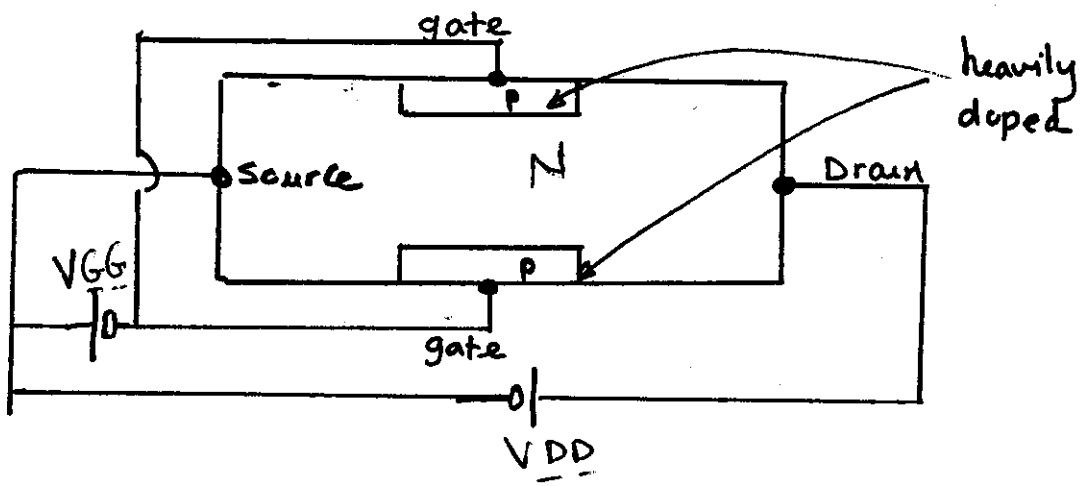
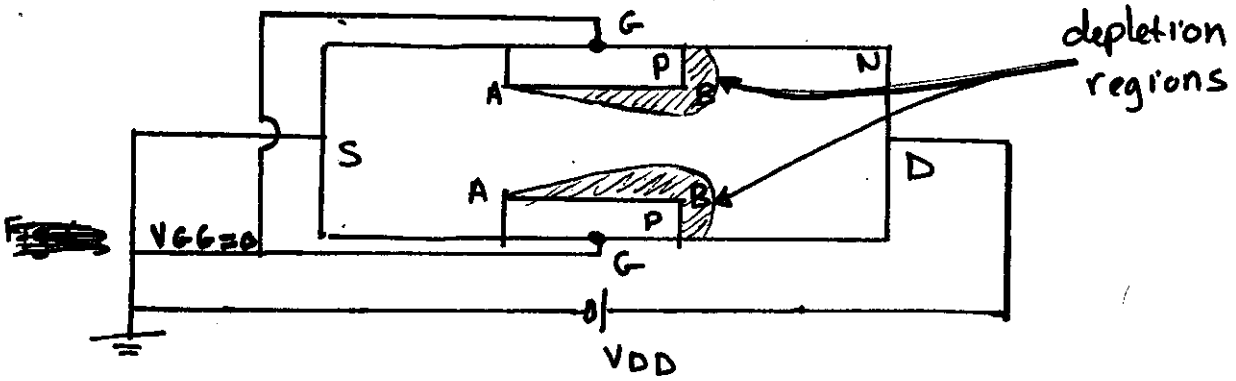


Fig 6.2

Let us first consider the operation of the JFET when $V_{GG} = 0$ as shown in the following diagram :



Since the P - layers are connected to zero voltage (ground) and because the layers are heavily doped , it follows that the voltages across the entire P regions are zero . Also , at the source end , the voltage is zero (because it is connected to ground) . i.e. the net voltage drop across the PN Junction , at points A equal zero (thus the depletion layer is very small at these points .

On the other hand , at points B , and while the voltage at the P - layer remains at zero level , the voltage at the Drain equals V_{DD}. i.e. the junctions at the locations B are reversed biased (thus large depletion layers forms). Of course , the width of such layers decreases as we move towards the A locations .
Initially , for a small V_{DD}, the depletion layer is small and the N - Channel is wide open and the current I_D is determined (linearly) by the resistance and cross

sectional area of the N - Channel and also by the level of doping of the material itself .
As V_{DS} increases , the depletion layer also increases , reducing the conductivity of the N - material (increasing its resistance) and reducing the voltage drop along the material . After some linear response , further increases in V_{DS} will result in reduction of the rate of I_D increases per unit increase in V_{DS} as illustrated in the Fig (6.3) :

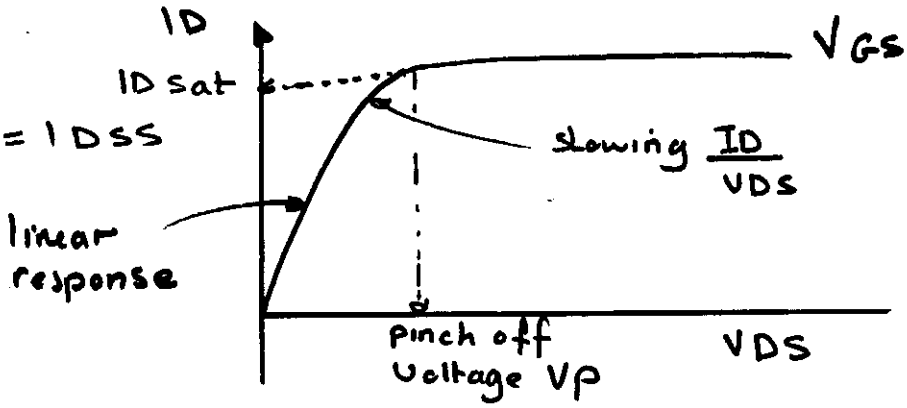


Fig 6.3

Eventually , a voltage V_{DS} is reached -- called the Pinch off voltage , V_P -- where by the depletion layers touch each other at the middle of the N - Channel , as shown in Fig (6.4) , and the current I_D reaches a maximum value (

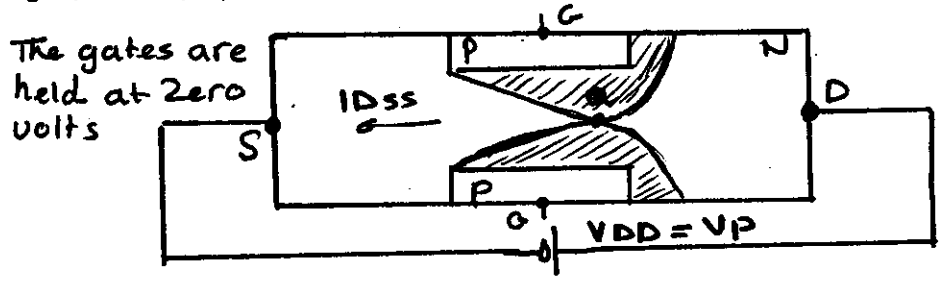


Fig 6.4

called , the saturation I_D or I_{DSS}, the saturation current (when V_{GS} is Short circuited) which is determined by the developed potential at point a .
Any further increases in V_{DS} will only thickens the depletion layer (the current driving potential , point a , remains at almost the same potential , leaving I_{DSS} unchanged) as shown in Fig (6.5) .

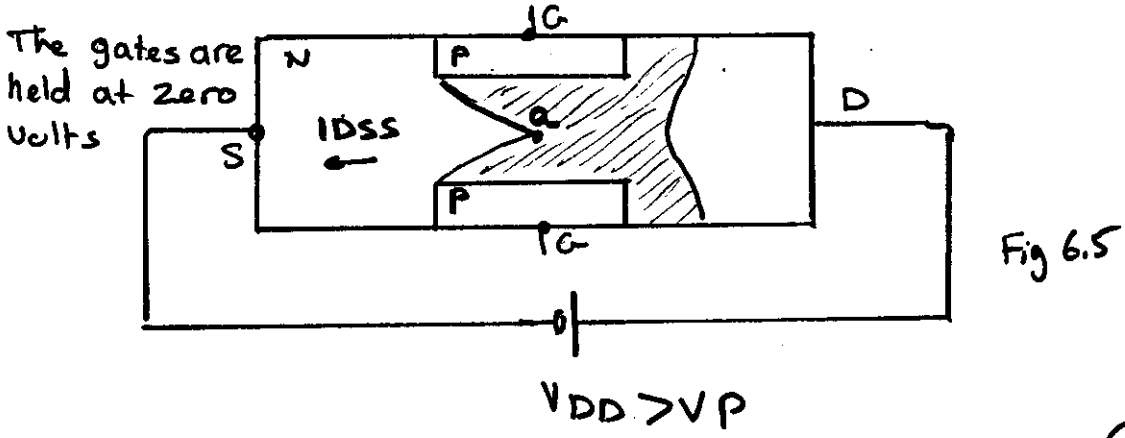


Fig 6.5

Now let us consider what happens if we apply a voltage V_{GS} .

It is clear that applying a negative V_{GS} would result in widening the initial depletion regions and thus a family of I_D verses V_{DS} curves for a variety of V_{GS} values can be obtained , as shown in Fig (6.6) .

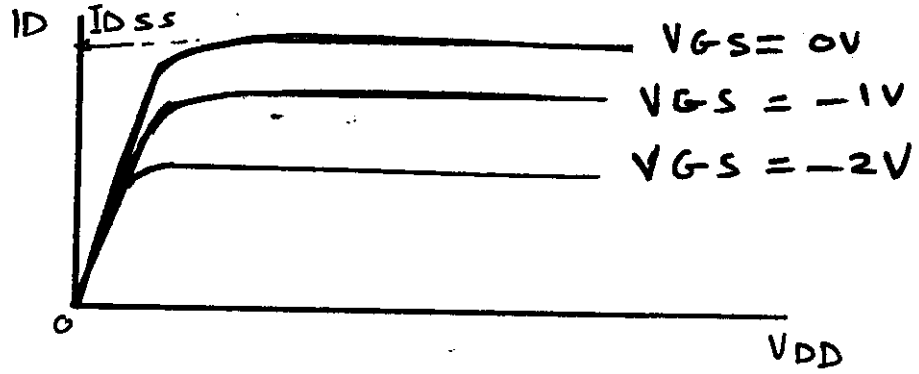


Fig 6.6

6.1.1.3 The transfer curve of the JFET

The characteristics of the JFET may also be displayed by a plot of I_D verses V_{GS} (output / input) . This is called the saturation transfer curve (for $V_{DS} >= V_P$, or the transition transfer curve (for $V_{GS} < V_P$ -- i.e. the linear regions). . Such curves may be constructed directly from the I_D , V_{DS} curves as shown in Fig (6.7).

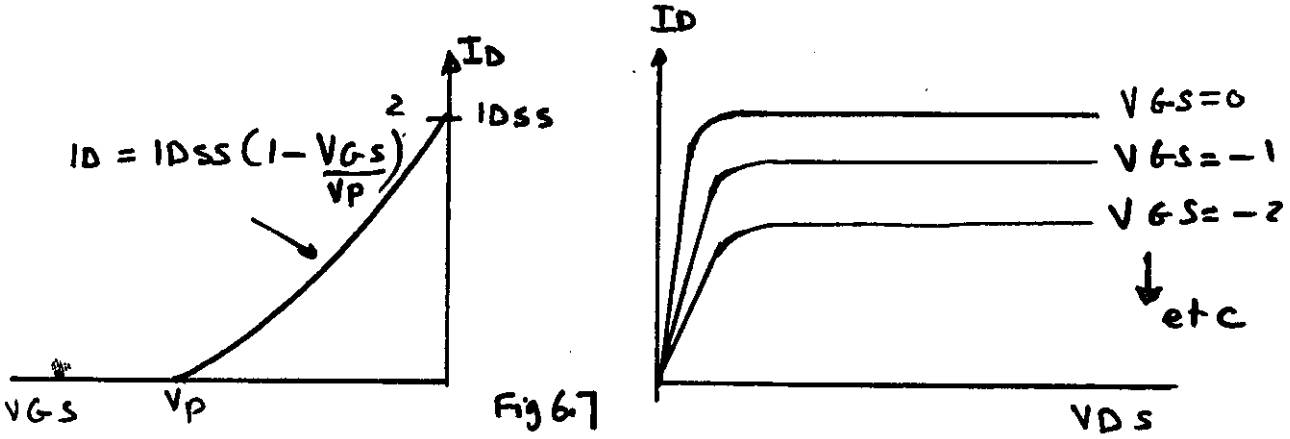


Fig 6.7

The mathematical relationship (see reference book for more details) which represent such response is as follows :

$$I_D = I_{DSS} \ (1 - V_{GS} / V_P)_2$$

6.1.1.4 The general JFET parameters .

I_{DSS} -- the saturation I_D at V_{GS} =0
V_P -- the Pinch off voltage
BV_{GSS} -- the FET breakdown voltage at V_{DS} =0
g_m -- the input conductance (semens) , given by

$$\Delta I_D / \Delta V_{GS} \text{ at } V_{DS} = 0$$

6.1.2 The MOSFET

6 .1.2.1 Types of MOSFET s

(a) Enhancement mode MOSFET (P or N Channel)

(b) Depletion mode MOSFET (P or N Channel)

6.1.2.1 The basic construction of the Enhancement mode MOSFET .

The basic construction of a N - Channel Enhancement Mode MOSFET (complementary semiconductor material for an P - Channel MOSFET is used) is as shown in Fig (6 .8) .

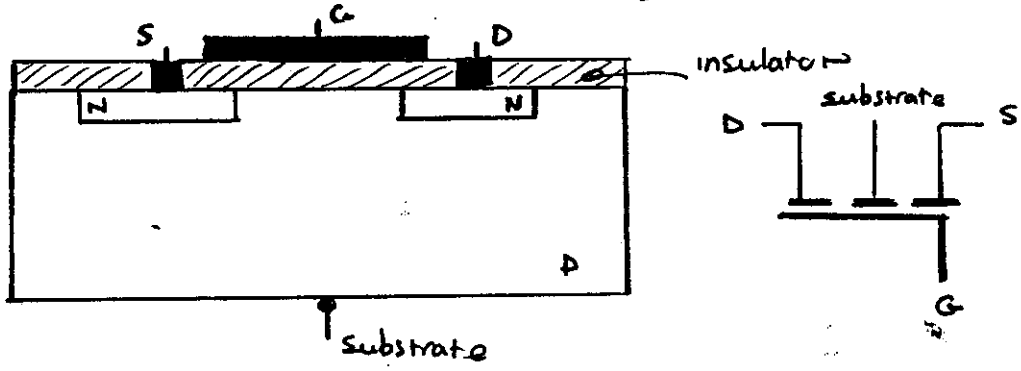


Fig 6.8

A P - substrate iused as the base substrate of the MOSFET . The Source and the Drain are connected , to two N - layers which are diffused on to the P - substrate . A metallic layer, deposited on the an insulating layer (called silicon dioxide), on the P - substrate and between the two N - layers is used as the gate of the MOSFET.
When a voltage V_{GS} is applied across the Gate and Source terminals , an N - Channel is induced as shown in Fig 6.9).

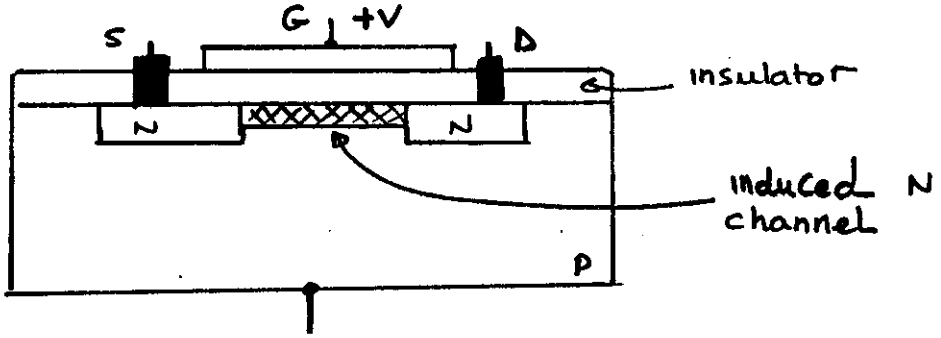


Fig 6.9

Under such condition and on applying a voltage V_{DS} across the Drain and Source terminals , I_D starts to flow. Initially ,such current increases ,linearly ,with V_{DS} , up

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const → construct of the device

$$I_D = K(V_{GS} - V_T)^2$$ switch on voltage

to a stage (similar to JFET) , called the Pinch off voltage , where by the induced N - Channel is pinched off as shown in Fig (6.10).

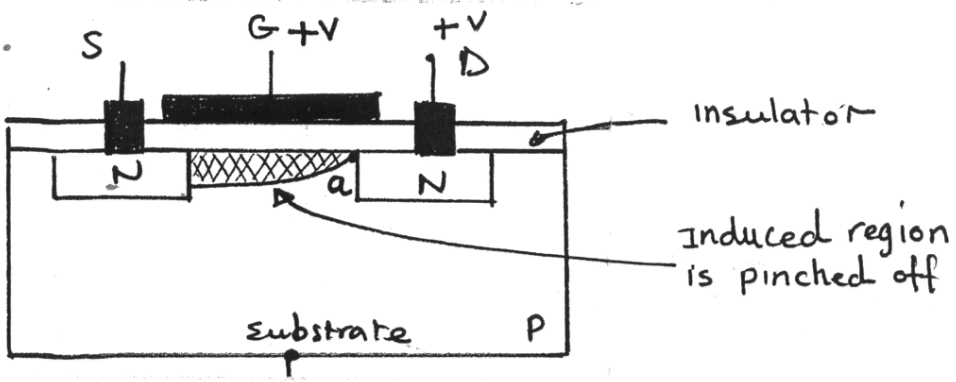


Fig 6.10

Any further increases in V_{DS} will not result in increases in I_D (i.e. I_D reaches it's saturation value).
The following curves depicts the characteristic curves for this type of MOSFET device .
It should be pointed out at this stage that V_{GS} should be above a certain voltage level (typically 2V) , in order to allow for the creation of the depletion layer and thus facilitating the I_D flow in response to increases in V_{DS} .

6.1.2.2 the Depletion mode MOSFET
considering an N - Channel depletion mode MOSFET , then the operation of this type of MOSFET will be similar to the enhancement mode MOSFET except in this case , the N - Channel is physically constructed on the P - substrate so that I_D can flow even if V_{GS} =0 (also for V_{GS} >0) . Also , to cut off the MOSFET (I_D =0 , for all values of V_{DS}) V_{GS} must go negative (typically - 5 V)

6.1.2.3 Complementary MOS --- CMOS

CMOS is a device made of P - Channel enhancement MOSFET and an N - Channel enhancement MOSFET connected into a complementary device . Such a device is very popular in digital circuits . Fig (6.11) illustrate the basic construction of the CMOS device . The two inputs of the PMOS and the NMOS (the two gates) are connected

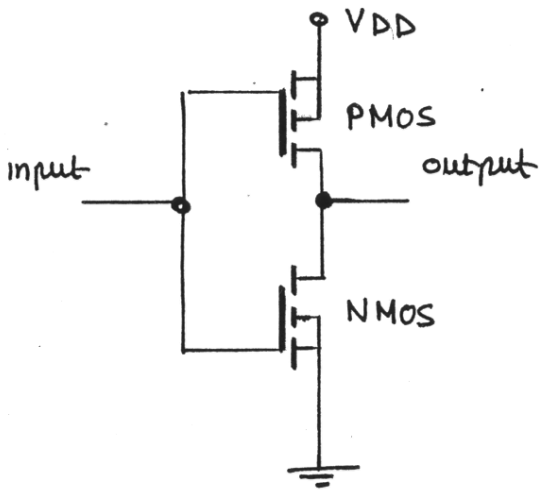


Fig 6.11

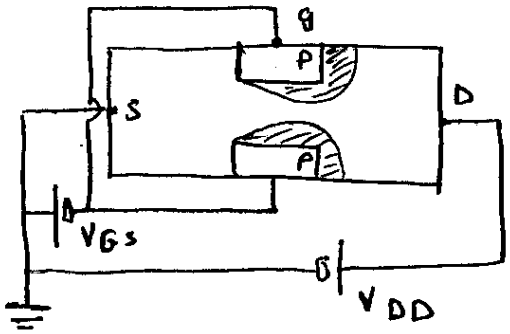
together to form a single input terminal . Also the two output source of PMOS and source of NMOS (or source and drain) are connected together to form a single output as shown in the above Fig .

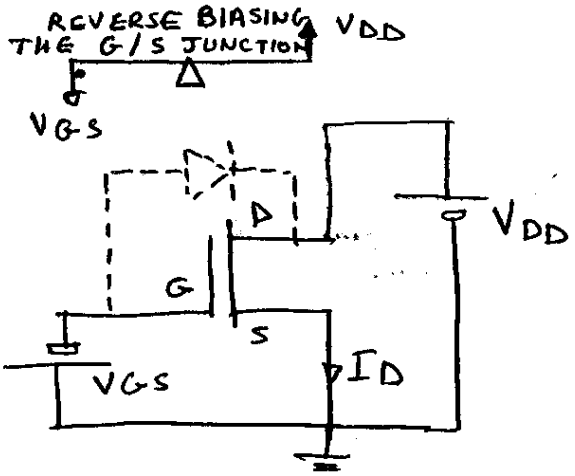
On applying a positive input to the common input terminal , the PMOS switches off and the NMOS switches on resulting in the output being driven to ground (zero voltage) . similarly , applying zero volt at the common input causes the PMOS to switch on and the NMOS to switch off which causes the output to be pulled up to VDD .

UMMARY of METHODS OF OPERATING FETS

ET:

N-channel





The depletion regions width can be increased (constricting the flow of current ID) by:

(a) Decreasing the value of VGS (negative)

(b) Increasing the value of VDD

(c) Both (a) and (b)

- Maximum ID is reached when the combined VGS and VDD cause the two depletion regions to meet each other at a point in the middle of the channel. i.e pinch off depletion region situation – VP (the voltage of VDD at pinchoff) is defined as VDD which will cause pinchoff of the depletion region /at VGS = 0

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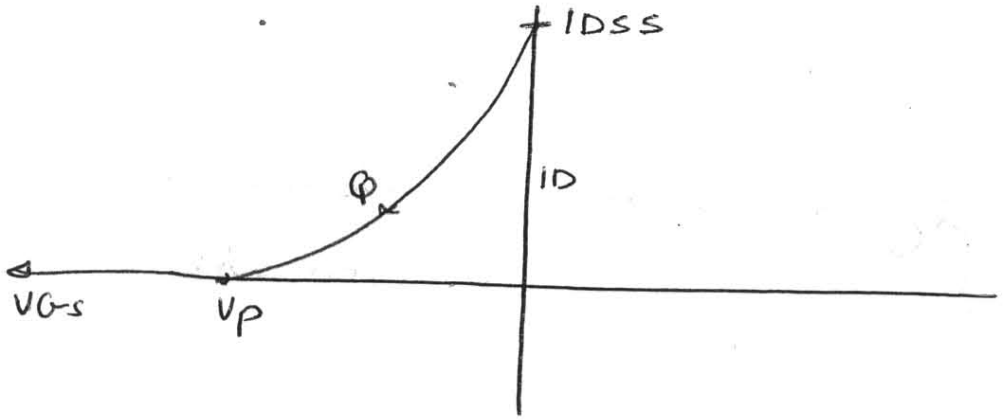
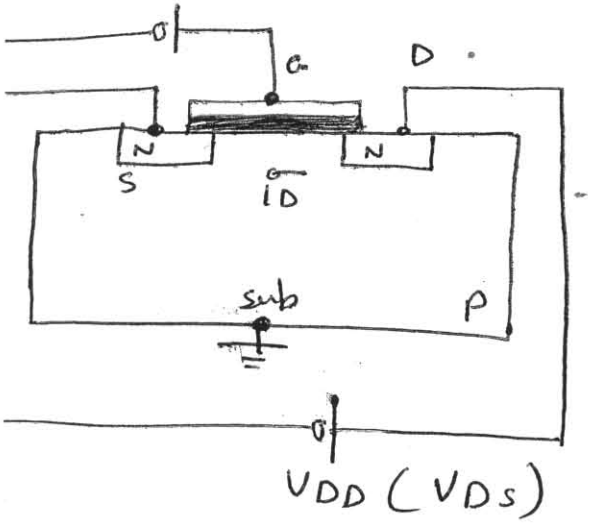
clearly, if VGS is Lowered below pinch off voltage value, then ID becomes Zero (no matter what value ~~is~~ VDD is) and the FET switches off

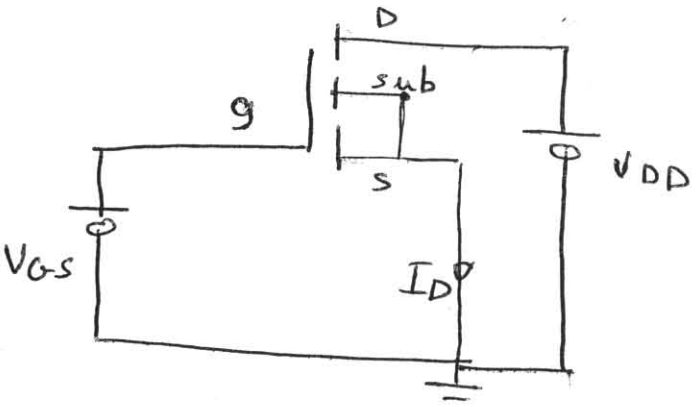
Biasing the JFET, therefore, can be done between VGS=0 and VGS = pinch off values



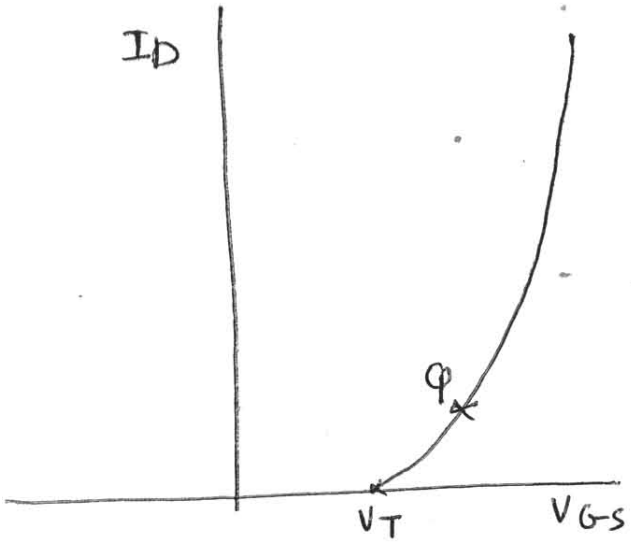
Note that if VGS is allowed to go positive, situation might arise where the gate/ source Junction becomes forward biased and urrent starts to flow between the gate nd source

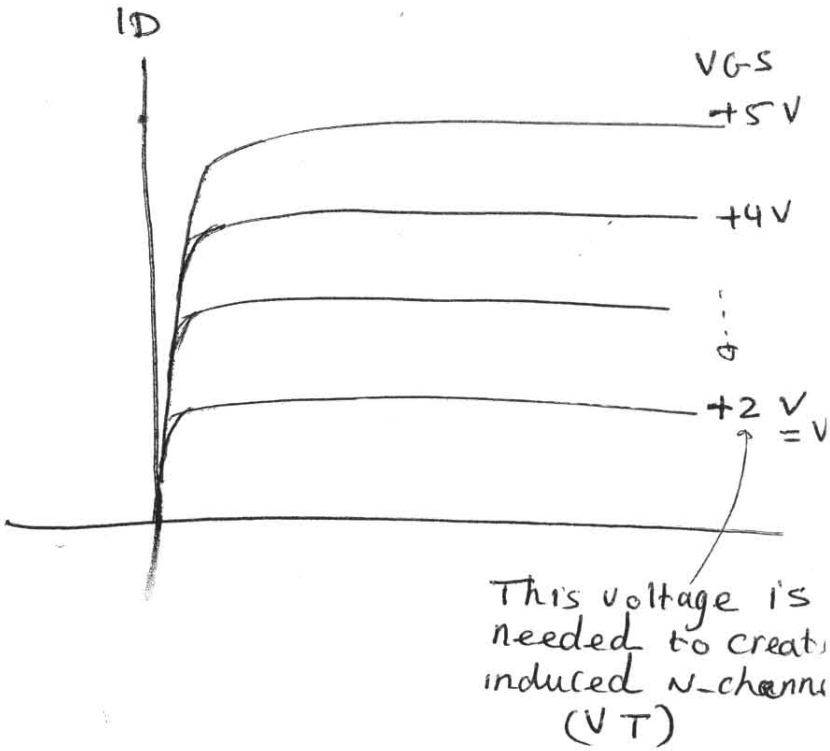
Enhancement MOSFET (N-channel)





- Induced, conducting, N-channel occurs when gate is made positive enough, V_T. The higher the gate voltage, the wider is the induced N-channel.
- Increasing V_{DS} causes a current I_D to flow along the induced ~~chan~~ channel, at the same time, constricting the induced N-channel, up to a stage where pinch off situation occurs





3- Biasing of enhancement FET should be made above V_T (which is the critical Gate voltage required to turn on the FET.)

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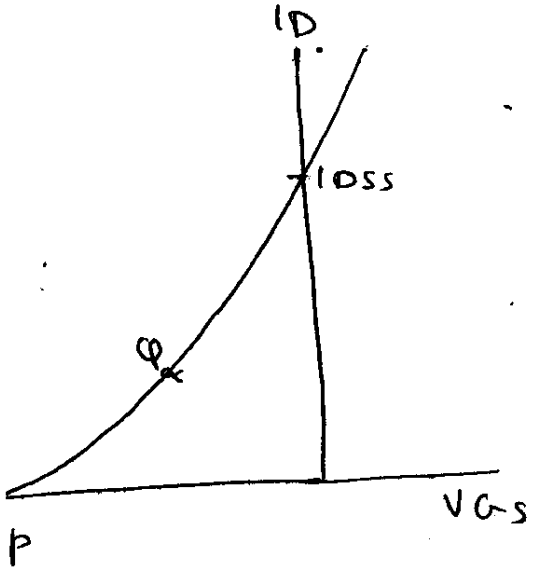
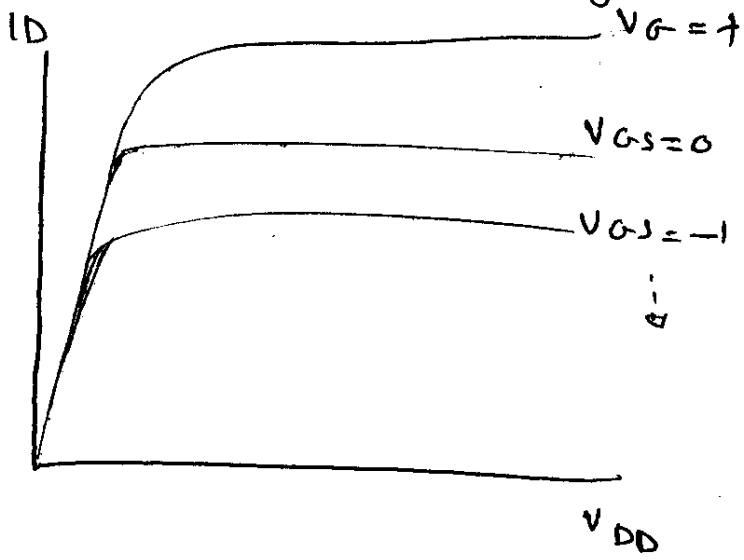
(11)

Depletion MosFET (N-channel)

VGS can be positive or negative – similar connection to the E-MosFET.

- Because the N-channel is physically present, then ID can flow even at zero VGS. Such a current can be enhanced if VGS is made positive [increases the concentration of electrons in the N-channel]
- when VGS is made negative, concentration of electrons in the N-channel is reduced decreasing the flow of ID





- Biasing this type of FET could be made any where above Vp

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